REMARKS

The following remarks are made in response to the Non-Final Office Action mailed January 11, 2006. Claims 32, 38 and 39 have been allowed. Claims 1-10 and 14-31 were rejected. Claims 11-13 have been objected to. With this Response, claims 14 and 30 have been cancelled and claims 1, 9, 20, 22, and 29 have been amended. Claims 1-13, 15-29, 31, 32, 38, and 39 remain pending in the application and are presented for reconsideration and allowance.

Claim Rejections under 35 U.S.C. § 112

Claims 9, 20, 22, and 29 were rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claims 9, 20, 22, and 29 have been amended. Applicant submits that amended claims 9, 20, 22, and 29 particularly point out and distinctly claim the subject matter which Applicant regards as the invention.

In view of the above, Applicant respectfully submits that the above rejection of claims 9, 20, 22, and 29 under 35 U.S.C. § 112, second paragraph, should be withdrawn. Allowance of claims 9, 20, 22, and 29 is respectfully requested.

Claim Rejections under 35 U.S.C. § 102

Claims 1-3, 5, 7-9, 14-16, and 20-31 were rejected under 35 U.S.C. § 102(b) as being anticipated by Moroni et al., U.S. Patent No. 5,606,531 ("Moroni"). Applicant submits that Moroni fails to teach or suggest the invention of amended independent claims 1, 9, 20, 22, and 29. Claims 14 and 30 have been cancelled.

Amended independent claim 1 recites a clock stop detector for a memory for detecting a clock signal being not active for a predetermined period of time. The clock stop detector comprises a first switch that closes in response to a first logic level of an inverted clock signal to charge a capacitor and a second switch that closes in response to a second logic level of the inverted clock signal to discharge the capacitor. The clock stop detector comprises a logic circuit

that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time. The capacitor is charged to the second logic level when the inverted clock signal is at the first logic level, and the capacitor is discharged to the first logic level when the inverted clock signal is at the second logic level for a period of time exceeding the predetermined period of time.

Moroni discloses an electronic device including a microprocessor, a circuit generating a clock signal, and memories incorporates a circuit for generation of a reset signal capable of detecting a stop in the oscillation of the clock signal and generating a logic signal coupled with the reset input of the microprocessor. The circuit monitors the clock signal applied to the device and, if an irregularity is detected, generates a reset signal holding the microprocessor in a safe state. The reset signal is held until the circuit generating the clock signal resumes normal operation. (Abstract).

The circuit block 2 has an input 13 connected to the terminal CK of the microcontroller and on which is applied the clock signal. The block 2 incorporates a circuit designed to detect clock signal irregularities. (Col. 3, lines 56-60). The input 14 of the block is connected to the control terminals of a first complementary pair of MOS transistors indicated by M1 and M2 and, through an inverting gate 15, to the control terminals of two other MOS transistors indicated by M5 and M6. Each pair of transistors is connected in series between a positive pole of the supply voltage generator Vcc and negative pole of the generator, i.e. to the circuit ground. (Col. 4, lines 27-34).

The drain terminals of the first pair of transistors M1 and M2 are connected together in the circuit node A and are also connected to a terminal of a first capacitor C1, to the drain terminal of a transistor M3 and to a first input of an AND logic gate 16. The second terminal of the first capacitor C1 is connected to the circuit ground. The drain terminals of the second pair of transistors M5 and M6 are connected together in the circuit node indicated by B and are also connected to a terminal of a second capacitor C2, to the drain terminal of a transistor M4 and to a second input of the logic gate 16. The second terminal of the second capacitor C2 is connected

to the circuit ground. The control terminals and source terminals of the two transistors M3 and M4 are both connected to the power supply line Vcc. The output terminal of the logic gate 16 constitutes the output 11 of the circuit block 2. (Col. 4, lines 45-62).

The clock signal present at the input 14 of the circuit takes into conduction the transistors M1 and M2 alternately. Consequently the circuit node A to which is also connected a terminal of the capacitor C1 is taken through the conduction resistances Ron1 and Ron2 of the two transistors M1 and M2 to the power supply voltage Vcc and to ground alternately. In this manner the capacitor C1 is charged and discharged alternately through the two resistances Ron1 and Ron2. By dimensioning the transistors M1 and M2 in such a manner that the transistor M2 has a conduction resistance Ron2 much greater than that of Ron1 of the transistor M1, at rated operation the capacitor C1 is charged to the power supply voltage Vcc and keeps high the logic level of an input of the logic gate 16. The input 14 of the circuit is also connected through an inverting gate 15 to the control terminals of the second pair of transistors M5 and M6. The function of these two transistors is similar to that of the two transistors M1 and M2 and is to keep the capacitor C2 charged at the power supply voltage Vcc and hence hold a second input of the logic gate 16 at a high logic level. The two transistors M5 and M6 are dimensioned in such a manner that the internal resistance Ron5 of the transistors M5 is much greater than that of Ron6 of the transistor M6. The output of the AND gate 16 is thus held at a high logic level during normal operation of the circuit. If the clock signal present on the input 14 of the circuit stops at a high or low logic level one of the two transistors M2 or M6 remains in a conduction state while discharging the capacitor to which its drain terminal is connected. If one of the two capacitors C1 or C2 is discharged, taking one of the two inputs of the logic gate 16 to a low logic level, the output of said gate changes state and passes from the high logic level to the low logic level. (Col. 4, line 63 – Col. 5, line 32).

Moroni fails to teach or suggest **a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time.** In contrast, Moroni discloses in Fig. 3 and in the associated

description that the logic circuit 16 receives a first charge signal from capacitor C1 and a second charge signal from capacitor C2, rather than a *clock signal* and a charge signal as recited in independent claim 1.

In view of the above, Applicant respectfully submits that the above rejection of independent claim 1 under 35 U.S.C. §102(b) should be withdrawn. Dependent claims 2, 3, 5, 7, and 8 further define patentably distinct independent claim 1. Accordingly, Applicant submits that these dependent claims are also allowable over the cited reference. Allowance of claims 1-3, 5, 7, and 8 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Moroni also fails to teach or suggest the invention of amended independent claim 9 including **a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time.**

In view of the above, Applicant respectfully submits that the rejection of claim 9 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 15 and 16 further define patentably distinct independent claim 9. Accordingly, Applicant submits that these dependent claims are also allowable over the cited reference. Allowance of claims 9, 15, and 16 is respectfully requested.

For similar reasons as discussed above with reference to claim 1, Moroni also fails to teach or suggest the invention of amended independent claim 20 including **means for providing a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time based on the clock signal and a charge signal based on a charge on the capacitor, the means for providing the control signal receiving the clock signal and the charge signal.**

In view of the above, Applicant respectfully submits that the above rejection of claim 20 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claim 21 further defines patentably distinct independent claim 20. Accordingly, Applicant submits that this dependent claim is also allowable over the cited reference. Allowance of claims 20 and 21 is respectfully requested.

For the same reasons as discussed above with reference to claim 1, Moroni also fails to teach or suggest the invention of amended independent 22 including **wherein the step of detecting the stopped clock signal comprises receiving the clock signal and the charge signal and detecting the stopped clock signal based on the received clock signal and the charge signal.**

In view of the above, Applicant respectfully submits that the above rejection of claim 22 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claims 23-28 further define patentably distinct independent claim 22. Accordingly, Applicant submits that these dependent claims are also allowable over the cited reference. Allowance of claims 22-28 is respectfully requested.

For similar reasons as discussed above with reference to claim 1, Moroni also fails to teach or suggest the invention of amended independent claim 29 including **a logic circuit that receives the clock signal and a charge signal based on a charge on the capacitor, and that outputs a control signal indicating when the clock signal was not active for a period of time exceeding the predetermined period of time.**

In view of the above, Applicant respectfully submits that the above rejection of claim 29 under 35 U.S.C. § 102(b) should be withdrawn. Dependent claim 31 further defines patentably distinct independent claim 29. Accordingly, Applicant submits that this dependent claim is also allowable over the cited reference. Allowance of claims 29 and 31 is respectfully requested.

Claim Rejections under 35 U.S.C. § 103

Claim 4 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Moroni et al. in view of Nakashima, U.S. Patent No. 5,517,144 ("Nakashima").

Claim 4 further defines patentably distinct independent claim 1. Accordingly, Applicant submits that this dependent claim is also allowable over the cited references. Allowance of claim 4 is respectfully requested.

Claim 6 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Moroni et al. in view of Forbes, U.S. Patent No. 6,649,476 ("Forbes").

Dependent claim 6 further defines patentably distinct independent claim 1. Accordingly, Applicant submits that this dependent claim is also allowable over the cited references. Allowance of claim 6 is respectfully requested.

Claim 10 was rejected under 35 U.S.C. § 103(a) as being unpatentable over Moroni et al. in view of Ooishi, U.S. Patent No. 6,246,614 ("Ooishi").

Dependent claim 10 further defines patentably distinct independent claim 9. Accordingly, Applicant submits that this dependent claim is also allowable over the cited references. Allowance of claim 10 is respectfully requested.

Claims 17-19 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Moroni et al.

Dependent claim 17-19 further define patentably distinct independent claim 9. Accordingly, Applicant submits that these dependent claims are also allowable over the cited references. Allowance of claims 17-19 is respectfully requested.

Allowable Subject Matter

The Examiner allowed claims 32, 38, and 39. The Examiner objected to claims 11-13 for being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all limitations of the base claim and any intervening claims. Claims 11-13 further define patentably distinct independent claim 9. Accordingly, Applicant submits that these dependent claims are also allowable over the cited references. Allowance of claims 11-13 is respectfully requested.

CONCLUSION

In view of the above, Applicant respectfully submits that pending claims 1-13, 15-29, 31, 32, 38, and 39 are in form for allowance and are not taught or suggested by the cited references. Therefore, reconsideration and withdrawal of the rejections and allowance of claims 1-13, 15-29, 31, 32, 38, and 39 is respectfully requested.

Amendment and Response
Applicant: Jungwon Suh
Serial No.: 10/804,840
Filed: March 19, 2004
Docket No.: I436.114.101/IO040310PUS
Title: CLOCK STOP DETECTOR

No fees are required under 37 C.F.R. 1.16(b)(c). However, if such fees are required, the Patent Office is hereby authorized to charge Deposit Account No. 50-0471.

The Examiner is invited to contact the Applicant's representative at the below-listed telephone numbers to facilitate prosecution of this application.

Any inquiry regarding this Amendment and Response should be directed to Steven E. Dicke at Telephone No. (612) 573-2002, Facsimile No. (612) 573-2005. In addition, all correspondence should continue to be directed to the following address:

Dicke, Billig & Czaja
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402

Respectfully submitted,

Jungwon Suh,

By their attorneys,

DICKE, BILLIG & CZAJA, PLLC
Fifth Street Towers, Suite 2250
100 South Fifth Street
Minneapolis, MN 55402
Telephone: (612) 573-2002
Facsimile: (612) 573-2005

Date: April 11, 2006
SED:mlm

Steven E. Dicke
Reg. No. 38,431

CERTIFICATE UNDER 37 C.F.R. 1.8:

The undersigned hereby certifies that this paper or papers, as described herein, are being transmitted via facsimile to Facsimile No. (571) 273-8300 on this 11 day of April, 2006.

By: Steven E. Dicke
Name: Steven E. Dicke